Status of Demonstrator Test System

E. Charles, K. Dao, K. Einsweiler, D. Fasching, J. Richardson
LBNL and Wisconsin

Summary of status of PLL production and testing

Summary of recent PixelDAQ software work

PLL Production and Testing

First production of 8 PLL's complete

- Presently 3 at CERN (2 in testbeam, one in pixel lab)
- Three others working (one each in LBL, Bonn, Genova)
- Two others not yet operational (one fixed yesterday...)
- Proposed distribution: Bonn, CERN, Genova, 2*LBL + 3 others

Next round of production launched (8 additional modules):

- Would expect to complete fabrication in 2-3 months

Present list of test system requests (15 modules total):

Albany, Bonn, CERN pixel lab, CPPM, Dortmund, Genova, Milano, New Mexico, Oklahoma, Ohio State, Toronto, Udine, Wuppertal

Operation of PLL requires:

- PC with VME and GPIB interfaces, preferably both from National Instruments
- LabWindows software version 5
- Total investment about 10K$ plus VME crate.

PLL firmware approaching a first complete release:

- Supports FE-A, FE-B, and FE-C single chips
- Supports MCC Replacement and full MCC (still under development with Genova)
- Supports LBL and Siegen PCC
- TFIFO now ready (100 μs playback of strobe/trigger/sync sequence).
- FPGA utilization just over 70%, but timing is fairly critical, so operation above 40 MHz is not really possible (board is synchronously clocked by master clock). Higher speed-grade FPGAs not available in compatible package (would require switch to BGA rather than QFP, so new PC board layout).

PixelDAQ Status

LabWindows software status:

- Supports complete set of scan operations (up to 2D), including FE DACs, PCC devices (DAC and delay), external GPIB devices, etc.
- Supports either internal trigger, or external (LEMO or Hitbus) trigger.
- Supports MCC replacement chip and first pass at full MCC chip.
- Supports first pass at module operation. Initializes registers for all enabled chips each time Run is started, including Command Register, Global Register, DAC Register, Pixel Register, and TDAC settings. Capable of doing a sequential scan of complete module (one chip at a time). User controls adresses of chips, plus which chips on module are initialized, and which are scanned.
- Supports realtime “hitmap” plotting of raw data, plus storage of all useful results in ASCII files which feed FORTRAN+CERNLIB analysis software for threshold scan, TOT calibration, timewalk scan, and source calibration.
- Source available on web for easy updating to new versions.